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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,197	04/09/2004	Tetsuji Yamaguchi	0756-7288	8599

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EXAMINER	
PERKINS, PAMELA E	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,197	YAMAGUCHI ET AL.	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-13 and 15-22* is/are allowed.

6)☒ Claim(s) *8,14 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/9/04, 12/12/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the election on 12 December 2005. Claims 8-22 are pending; claims 1-7 and 23 have been cancelled.

Election/Restrictions

Applicant's election without traverse of group II, claims 8-22 in the reply filed on 12 December 2005 is acknowledged.

Claims 1-7 and 23 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected group I, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 12 December 2005.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seo et al. (6,841,433) in view of Clevenger et al. (6,777,286).

Seo et al. disclose a method for manufacturing a thin film transistor where a semiconductor film (102) is formed over an insulating substrate (100); forming a first insulating film (104) over the semiconductor film (102); heat-treating the semiconductor

film and the first insulating film (Fig. 3B; col. 6, lines 37-49); patterning the semiconductor film (102) and the first insulating film (106) into island shapes (107) with the use of the same photomask after heat-treating the semiconductor film and the first insulating film to form an island-shaped semiconductor film and an island-shaped gate insulating film (107); forming a conductive film (112) over the island-shaped gate insulating film after forming the side wall; and patterning the conductive film to form a gate electrode (col. 7, lines 34-44).

Seo et al. do not disclose forming a second insulating film over the island-shaped gate insulating film; etching the second insulating film anisotropically to form a side wall covering side faces of the island-shaped semiconductor film and the island-shaped gate insulating film in self-aligned manner.

Clevenger et al. disclose a method for manufacturing a thin film transistor where a semiconductor film (10) is formed over an insulating substrate (20; patterning the semiconductor film (10) to form an island-shaped semiconductor film; forming a insulating film (80) over the island-shaped gate insulating film; etching the insulating film anisotropically to form a side wall (70) covering side faces of the island-shaped semiconductor film in self-aligned manner; forming a conductive film (85) over the island-shaped gate insulating film after forming the side wall; and patterning the conductive film to form a gate electrode (col. 5, lines 43-59).

Since Seo et al. and Clevenger et al. are both from the same field of endeavor, a method for manufacturing a thin film transistor, the purpose disclosed by Clevenger et al. would have been recognized in the pertinent art of Seo et al. Therefore, it would

have been obvious to one of ordinary skill in the art at the time the invention was made to modify Seo et al. by forming a insulating film over the island-shaped gate insulating film; etching the insulating film anisotropically to form a side wall covering side faces of the island-shaped semiconductor film in self-aligned manner as taught by Clevenger et al. to reduce leakage (col. 1, line 66 thru col. 2, line 29).

Referring to claims 14 and 16, Seo et al. do not disclose the heat-treating the semiconductor film and the first insulating film is done at a temperature of from 600 ^{O}C to 800 ^{O}C and wherein a strain point of the insulating substrate is equal to or lower than 600 ^{O}C. It would have been obvious to one having ordinary skill in the art at the time invention was made to heat-treat the semiconductor film and the first insulating film is done at a temperature of from 600 ^{O}C to 800 ^{O}C and wherein a strain point of the insulating substrate is equal to or lower than 600 ^{O}C disclosed in the claimed invention, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

Allowable Subject Matter

Claims 9-13 and 15-22 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: referring to claims 9 and 12, prior art does not anticipate, teach, or suggest insulating a side face of the semiconductor film by adding oxygen or nitrogen to a side face of the island-shaped semiconductor film without removing the resist mask.

Referring to claims 10 and 13, prior art does not anticipate, teach, or suggest forming a second insulating film over the island-shaped gate insulating film; patterning the second insulating film to cover edge portions of the island-shaped semiconductor film and the island-shaped gate insulating film and only a peripheral portion of a top face of the island-shaped gate insulating film.

Referring to claim 11, prior art does not anticipate, teach, or suggest forming a first insulating film over the semiconductor film; forming a first conductive film over the first insulating film; heat-treating the semiconductor film, the first insulating film, and the first conductive film; forming a second insulating film over the first island-shaped conductive film; and etching the second insulating film anisotropically to form a side wall covering side faces of the island-shaped semiconductor film, the island-shaped gate insulating film, and the first island-shaped conductive film in a self-aligned manner.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sekiya (JP04-139882) disclose a second insulating film formed at the side wall covering side faces of the island-shaped semiconductor film and the island-shaped gate insulating film in self-aligned manner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

Zandra V. Smith
Supervisory Patent Examiner
20 March 2006